**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) For testing semiconductor devices, a digital testing system comprising:

a test module including:

pattern memory for storing test vectors adapted for performing digital tests;

a digital test engine for implementing test vectors of the pattern memory, whereby digital inputs are provided to a device under test (DUT) and digital DUT outputs are captured, thereby testing the operability of the DUT[[.]]; and

a multiplexer for interfacing the DUT with an automatic test equipment (ATE) operably connected to perform testing on the DUT.

2-3. (canceled)

4. (original) A digital testing system according to claim 1 configured to perform mixed signal testing.

5. (original) A digital testing system according to claim 1 configured to perform scan testing.

6. (original) A digital testing system according to claim 1 configured to perform functionality testing.

7. (currently amended) A digital testing system according to claim [[3]] 1 wherein the testing module comprises a hardware device.

8. (currently amended) A digital testing system according to claim [[3]] 1wherein the testing module comprises firmware.

9. (original) A digital testing system for adding digital test capability to an automatic test equipment (ATE) platform, the system comprising;

automatic test equipment (ATE) adapted for performing analog testing of a device under test (DUT); and

a testing module further comprising pattern memory, a test engine, and a multiplexer for interfacing the DUT with the automatic test equipment (ATE), for performing digital testing on the DUT.

10. (original) A digital testing system according to claim 9 wherein the testing module further comprises DDR SRAM.

11. (original) A digital testing system according to claim 9 wherein the testing module further comprises an FPGA.

12. (original) A digital testing system according to claim 9 wherein the testing module further comprises a high speed bus.

13. (currently amended) A digital testing system according to claim 9 configured to perform [[scan]] mixed signal device testing.

14. (original) A digital testing system according to claim 9 configured to perform scan testing.

15. (original) A digital testing system according to claim 9 configured to perform functionality testing.

16. (original) A method for digital testing of a semiconductor device under test (DUT) positioned in a socket on a device interface board (DIB) including a test module, the method comprising the steps of:

storing test vectors for performing tests in machine-readable memory;

using the test vectors, providing digital inputs to the DUT; [[and]]

capturing and comparing digital DUT outputs, thereby determining the operability of the DUT[[.]] and

multiplexing the DUT between the test module and an automatic test equipment (ATE).

17. (canceled)

18. (currently amended) A method according to claim 16 further comprising the step of using the automatic test equipment (ATE) for testing analog properties of the DUT.

19. (original) A method according to claim 16 wherein determining the operability of the DUT further comprises the step of scan testing.

20. (original) A method according to claim 16 wherein determining the operability of the DUT further comprises the step of functionality testing.

21. (original) A method according to claim 16 wherein determining the operability of the DUT further comprises the step of mixed signal testing.